Modeling and PSPICE Simulation of NBTI Effects in VDMOS Transistors

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Abstract: In this paper the results of modeling and simulation of NBTI effects in p-channel power VDMOS transistor have been presented. Based on the experimental results, the threshold voltage shifts and changes of transconductance during the NBT stress have been modeled and implemented in the PSPICE model of the IRF9520 transistor. By predefining the threshold voltage value before the NBT stress, and by assigning the stress time, transfer characteristics of the transistor are simulated. These characteristics are within (1.33÷11.25)% limits in respect to the measured ones, which represents a good agreement.

Keywords: NBTI, Modeling, PSPICE simulation, VDMOS transistor.

1   Introduction

Many investigations are dedicated to the modeling and PSPICE simulation of effects generated by various external influences which degrade characteristics of semiconductor devices. Two major approaches for the implementation of these degradation effects into PSPICE models can be distinguished. The first one is modification of the existing model parameters based on the experimental results (model parameters extraction) [1 – 3]. The second approach is addition of the specific elements into the basic circuit of the modeled device. In the latter case, the additional element is, most commonly, parametrically controlled voltage source. Values of the controlling parameters are functions of the modeled external influence (e.g. value of the control parameter is function of the electrical or radiation stress time) [4 – 6]. It should be noted that these two approaches are not opposed to each other, but complementary, and their combination provides correct modeling of degradation effects.

NBTI (Negative Bias Temperature Instability) effects in semiconductor devices are known for a long time, but they have become more significant with

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the development of MOS technologies and decrease of the gate oxide thickness [7]. Despite the continuous study of NBTI effects and recognition of their impact on the electrical characteristics of MOS transistors, mechanisms responsible for these degradations are still not completely known. This is the reason why many scientists are nowadays oriented to the intensive investigation of the NBTI in MOS transistors [8] – [10].

In this paper is presented procedure for PSPICE modeling of NBTI effects in p-channel power VDMOS transistor IRF9520 [11] by combined approach. In these devices NBTI effects occur when they are exposed to temperatures in the range $(100 - 250)°C$ and gate oxide electric field of $(2 - 6)$ MV/cm. NBTI effects cause a decrease of transconductance (g_m) and saturation drain current (I_{Dsat}), as well as an increase of threshold voltage (V_T) and absolute "off" current (I_{off}) of the transistor. Influences of degradation effects on the threshold voltage and transconductance values are considered here.

2   Modeling of NBTI Effects

2.1 Experimental results

Measured values of voltage and current in the saturation regime of IRF9520 transistor are used for PSPICE model setup. Obtained experimental transfer characteristics are set as reference for fitting procedures and comparison of simulation results. Fig. 1 shows experimental transfer characteristics of transistor during NBT stressing at negative gate voltage of $V_{GS} = –40$ V (electric field in the oxide E ≈ 4 MV/cm) and temperature of 150°C. For measurement of the transfer characteristics during NBT stressing, the system presented in details in [12] is used.
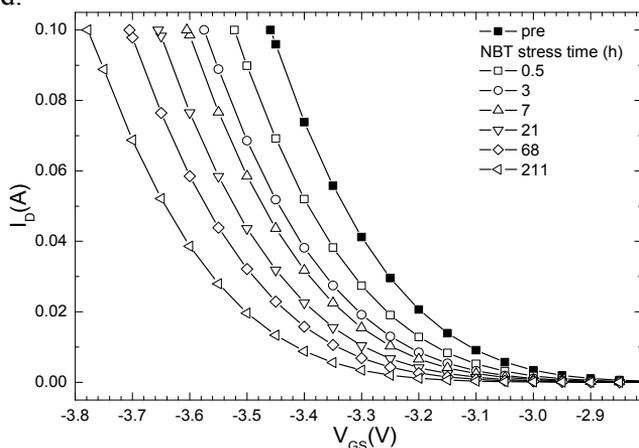

Fig. 1 – Experimental transfer characteristics of p-channel VDMOS power transistor IRF9520 during NBT stressing at V$_{GS}$ = –40 V and T = 150°C.

2.2 Modeling of the threshold voltage shift

VDMOS transistor IRF9520 is modeled in PSPICE as a subcircuit whose main part is PMOS transistor (level 1) [13]. During the model setup, threshold voltage is defined as the main electrical parameter of MOS transistor. The threshold voltage of commercial IRF9520 transistors is in the range from –2 V to –4 V [11], which makes difficult to generate an universal PSPICE model of this transistor. Based on the experimental results, for the threshold voltage value before NBT stressing (V_{T0}) is used value of –3 V.

For the threshold voltage shift during NBT stressing (ΔV_T), are responsible changes in densities of the oxide-trapped charge (ΔN_{ot}) and the interface traps (ΔN_{it}):

$$\Delta V_T = V_T - V_{T0} = -\frac{q}{C_{ox}}(\Delta N_{ot} + \Delta N_{it}),$$ (1)

where C_{ox} is capacitance of the gate oxide by cm². For the complete modeling of these shifts, a great number of parameters that define the voltage-temperature instabilities must be included. These parameters are: stress time and temperature, gate voltage, source-bulk voltage, gate oxide thickness, ratio of the channel width and length, frequency and duty cycle of the applied voltage pulses, as well as measurement speed. Parameters considered here are: stress time and temperature, gate voltage and gate oxide thickness. On the basis of the results published in [14], changes of N_{ot} and N_{it} (in cm⁻²), as a function of the electric field E (MV/cm), stress time t (h) and temperature T (K), are presented as:

$$\Delta N_{ot}(t) = AE^{2.44}t^{0.25}\exp(-0.21/kT),$$ (2)

$$\Delta N_{it}(t) = BE^{2.11}t^{0.18}\exp(-0.15/kT),$$ (3)

where A and B are fitting parameters, and k Boltzmann's constant.

The effect of NBT stressing is included in PSPICE by addition of the auxiliary voltage generator (VTH) into electrical schematics. Its value represents the threshold voltage shift according to (1), (2) and (3).

2.3 Modeling of the transconductance change

The second important parameter in the PSPICE model of PMOS transistor is transconductance parameter K_P [15]. It is defined as a product of the carrier mobility in the channel (μ) and the gate oxide capacitance (C_{ox}) which is proportional to the gate oxide thickness.

$$KP = \mu C_{ox}.$$ (4)

Transconductance value determines the slope of the transfer characteristic and, by tuning of this parameter, simulated and experimental characteristics are matched. For transconductance change modeling, direct modification of existing

PSPICE model parameters is performed. Namely, by iterative fitting of the simulated characteristics to the experimental ones, the value of K_P parameter is determined for different NBT stress times.

The parameter K_P can be extracted from measurement by two methods: as a slope of the transfer characteristic in the linear regime for low V_{DS} values, or as a slope of the $\sqrt{I_D} - V_{GS}$ characteristics in the saturation regime [16]. The values of K_P extracted by two methods will differ since the effect of mobility decrease due to the gate oxide electric field is not included. PSPICE allows to define only one K_P value for both operations regimes, which introduces an additional error into the simulation results.

2.4 PSPICE simulation of NBTI effects

The simulation of NBTI effects in power VDMOS transistors IRF9520 in program PSPICE is realized following the experimental procedure where continual temperature-voltage stressing was periodically interrupted for electrical characterization of the transistor [14]. Established simulation procedure does not have "memory effect", i.e. after determination of the transfer characteristic for the particular NBT stress time, there is no subsequent stressing. This is the reason that, for each transfer characteristic (each defined stress time), it is necessary to simulate NBT stressing from the zero moment. The first part of the simulation represents the NBT stressing, while the second is characterization – generation of the transfer characteristic. Results of the first simulation part are input parameters for the second one. Simple flowchart of the PSPICE simulation is presented in Fig. 2a.

In Fig. 2b is presented electrical schematics implemented in PSPICE. Voltage generator VTH in the model of IRF9520 transistor defines the threshold voltage shift due to the stress. Transistor is configured to operate in the saturation region for simulation of the $I_D = f(V_{GS})$ characteristics. Value of the voltage V_{in} in simulation was in the range of 0 to –3.8 V.

3   Results and Discussion

By using PSPICE command **.FUNC**, whose parameter is time, changes of N_{ot} and N_{it} for the specific values of the oxide electric field and stress temperature are determined according to (2) and (3). Value of the parametrically controlled auxiliary voltage generator VTH is function of ΔN_{ot} and ΔN_{it} according to relation (1). By setting the simulation time through PSPICE **.TRAN** directive NBT stress time is included. The result of the simulation is threshold voltage shift (ΔV_{TH}) after NBT stressing. Fig. 3 presents threshold voltage shift (ΔV_{TH}) during the stress of 211 h. Results are obtained for oxide electric field of $E = 4$ MV/cm, temperature of $T = 150°C$, and parameters $A = 1.55 \cdot 10^{11}$ and $B = 1.11 \cdot 10^{10}$. Threshold voltage increases by the absolute

value compared to the value before stressing, and after 211 h this shift is 0.295 V. Results of the simulation are in accordance with the experimental data given in [14].
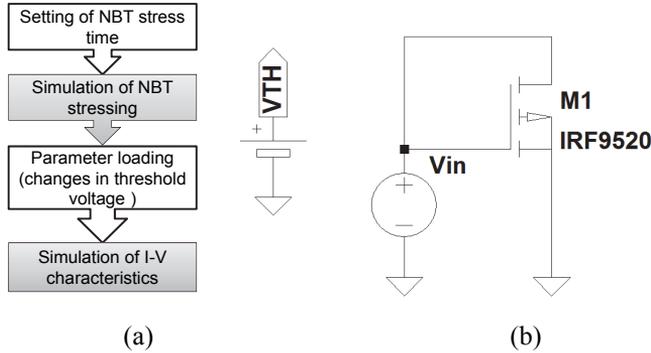

(a)   (b)

Fig. 2 – *(a) Flowchart of the PSPICE simulation of NBT stressing and generation of the transfer characteristics; (b) Electrical schematics of VDMOS transistor IRF9520 with auxiliary voltage generator VTH for simulation of the transfer characteristics.*
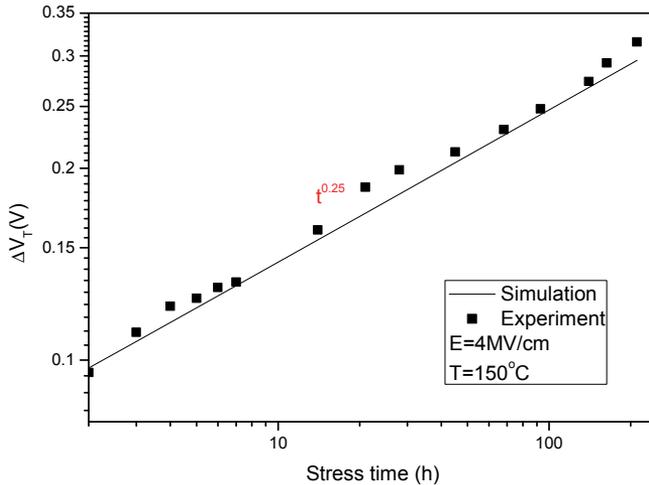

Fig. 3 – *Threshold voltage shift vs. NBT stress time obtained by simulation and experimentally.*

It should be noted that dependence of the threshold voltage shift of p-channel power VDMOS transistor IRF9520 on stress time, as given by (2) and (3), follows the law t^n. Depending on the value of parameter n, three different phases can be distinguished [7],[13], [17]]. In the first and third phase parameter n depends considerably on the applied voltage and temperature, while in the second phase it is almost constant with the value of 0.25. This value of parameter n is found in numerous investigations of NBTI in *p*-channel MOS

transistors realized in different technologies [18]–[21], and it is related to the dominant role of ΔN_{ot} over ΔN_{it}. Beginning of the second phase during the stressing is sooner as voltage and/or temperature are increased. In rigid stress conditions (high voltages and/or temperatures), it is possible that the first phase doesn't occur at all. Since this paper presents initial results of the simulation of NBTI effects in p-channel power VDMOS transistors, only the second phase is considered, i.e. the threshold voltage shift depends on the stress time as $t^{0.25}$.

Obtained value of the threshold voltage shift is used as input parameter in PSPICE netlist for generation of the transfer characteristics. By iterative fitting of the simulated onto the experimental characteristic, value of the parameter K_P is determined. It reflects the influence of transconductance changes on the transistor characteristics. Fig. 4 presents measured and simulated transfer characteristics of transistor IRF9520 before and after 211 h of stressing, at gate voltage of $V_{GS} = -40$ V and temperature of $T=150°C$. It is evident that, when transconductance change is not included by parameter K_P, there is a significant difference between measured and simulated characteristics. Appropriate adjustment of the K_P value enables good matching of these characteristics.
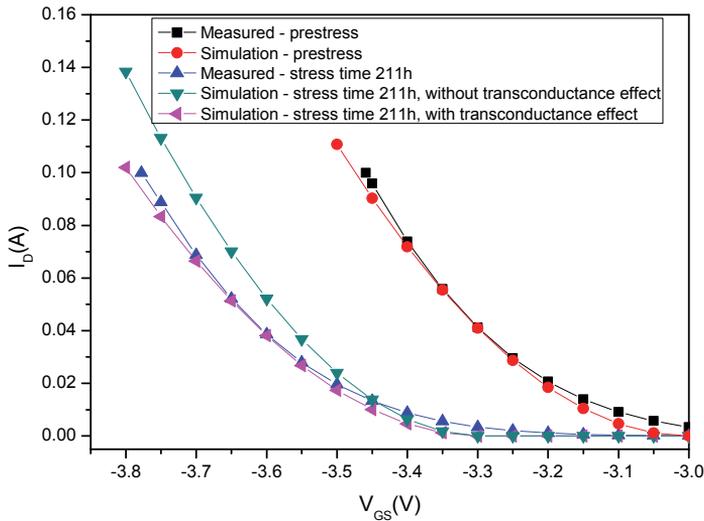

Fig. 4 – *Experimental and simulated transfer characteristics of transistor IRF9520 before and after the stress of 211 h, at $V_{GS} = -40$ V and $T = 150°C$.*

Parameter K_P, from the value before stressing ($2.74 \cdot 10^{-5}$ A/V^2), decreases up to 30% after the stress of 211h. On the other hand, it is experimentally determined that carrier mobility in the channel decreases for maximum 10% during 211 h of stressing [13]. As an illustration, in Fig. 5 are shown fitted values of the parameter K_P and normalized experimental values of the carrier

mobility during the stressing. It can be concluded that the appropriate value of the parameter K_P includes not only the effect of changes in mobility, but also additional effects. Dependence of the fitted values of K_P parameter on the stress time is approximated by the relation:

$$K_P = \frac{1}{a + bt^c},$$
(5)

where parameters have values: $a = 0.3377$, $b = 0.0902$, $c = 0.1284$. Ratio of the parameter K_P and normalized mobility (μ/μ_0) determines correction factor, whose dependence on the stress time is given in Fig. 6.
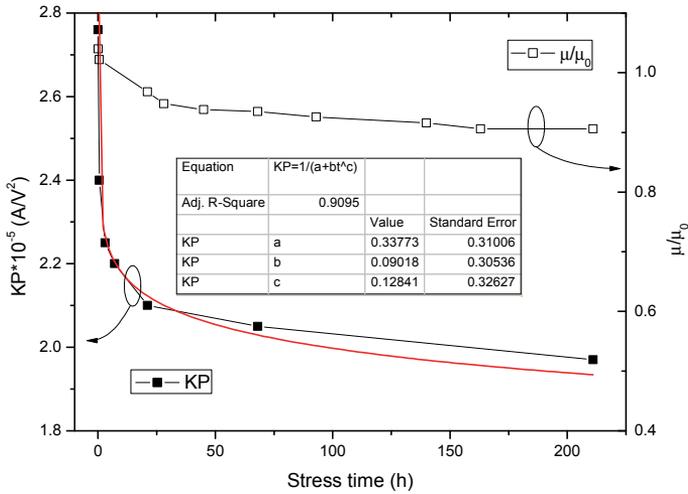

Fig. 5 – *Dependence of the parameter K_P and normalized mobility on the stress time.*

Values of PSPICE model parameters V_{T0} and K_P for characteristic NBT stress times used in simulations are given in **Table 1**. Value of the parameter V_{T0} for the specific stress time is sum of the threshold voltage before and its shift after the stress. In Fig. 7 are shown relative errors of the simulated drain current comparing to the experimental values as a function of the gate voltage (Fig. 4). The relative error before the stress is in the range (0.48–5.81)% for gate voltages above the threshold. However, in the subthreshold region, the error is even 100%. Discrepancies are considerable (22.05÷35.06%) when change in transconductance with stress time is not included. By adjusting the parameter K_P the error is significantly reduced (1.33÷11.25)%. Also, from the Fig. 7, it is obvious that there is a good agreement between simulated and experimental characteristics in the region above the threshold voltage, but for the subthreshold region this is not the case. The proposed model should be extended for simulation of NBTI effects in the subthreshold region.
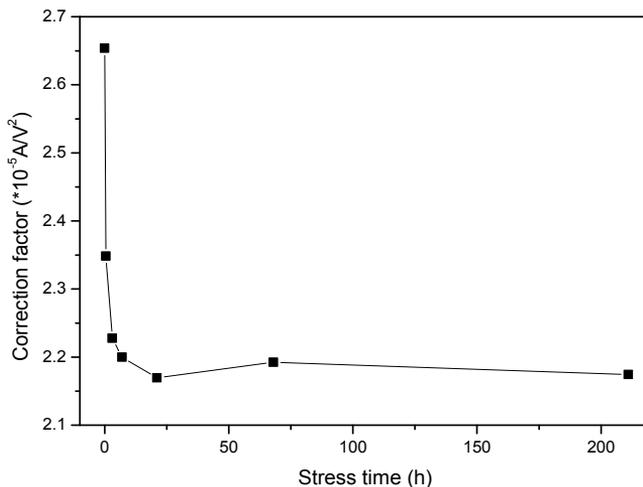
Fig. 6 – *Correction factor vs. NBT stress time.*

Table 1
Values of PSPICE parameters V_{T0} and K_{P0} for different NBT stress times.

Stress time (h)	V_{T0} [V]	$K_P \cdot 10^{-5}$ [A/V^2]
0	−3.0	2.74
0.5	−3.06996	2.40
3	−3.10692	2.25
7	−3.13079	2.20
21	−3.16995	2.10
68	−3.22510	2.05
211	−3.29535	1.97

4   Conclusion

Results of the modeling and PSPICE simulation of NBTI effects in p-channel power VDMOS transistors IRF9520 are presented. Based on the experimental data, threshold voltage shifts and transconductance changes due to NBT stressing are implemented into PSPICE model of the transistor. Threshold voltage shift is modeled by auxiliary parametrically controlled voltage generator, while the transconductance change is defined by model parameter K_P. Values of the K_P as a function of the stress time are determined by fitting of the simulated and experimental transfer characteristics. Appropriate analytical

approximation of this dependence is proposed. Based on the threshold voltage value before the stress, by setting the stress time, proposed model give transfer characteristics which are close to the experimental ones. Difference is in the range 1.33% to 11.25% in the region above the threshold. The main drawback of the proposed model is inability to model subthreshold characteristics, and this will be included in the future investigations. It is planned to investigate influence of the oxide electric field and temperature onto the threshold voltage shift and to establish overall model of p-channel VDMOS power transistors with NBT stress effects.
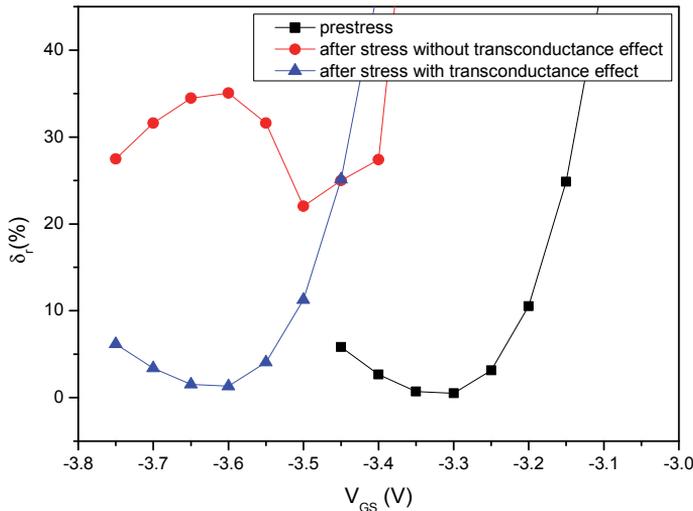

Fig. 7 – *Relative error of the simulated drain current compared to experimental values vs. gate voltage V_{GS}.*

5 Appendix

PSPICE netlist for determination of the threshold voltage shift at $E = 4$ MV/cm and $T = 150°C$ (the time variable TIME is in seconds):

```
.options numdgt=8 reltol=0.01 itl2=120 stepgmin gmin=1e-16
.FUNC Not() {1.44e10*pwr(TIME/3600,0.25)}
.FUNC Nit() {3.4e9*pwr(TIME/3600,0.18)}
E1 1 0 VALUE={-4.63e-12*(Not()+Nit())}
.TRAN 1 759600 uic
.probe v(1,0)
.print tran v(1,0)
.SAVEBIAS "napon.bsp" TRAN TIME=759600
.END
```

PSPICE model of PMOS transistor in subcircuit of IRF9520 [10] transistor which is modeled:

```
  .MODEL  MM  PMOS  LEVEL=1  IS=1e-32  L=2.5u  W=105000u  +VTO={-3+VTH}
LAMBDA=0.01 KP=1.97e-5 CGSO=3.45033e-4 +CGDO=1e-11
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6   Acknowledgment

7   References

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